insulating layer being formed outside the dummy pattern but not being formed over the dummy pattern.

REMARKS

The Examiner's Office Action of December 3, 2002 has been received and carefully reviewed. Claims 1, 27, 29 are amended. Claims 21-26 have been withdrawn from consideration. Thus, claims 1-20 and 27-33 are pending in this application. For at least the following reasons, it is submitted that this application is in condition for allowance.

In the Action, the amendment filed September 10, 2002 is objected to under 35 U. S. C. 132 because it introduces new matter into the disclosure. The examiner specifically points out that "a peripheral are where an integrated circuit is not formed, the peripheral area surrounding the circuit" is not supported by the original disclosure. The limitation in claim 1, 27 and 29, which was added into the claim by the amendment filed September 10, 2002 and which relates to the above-mentioned phrase, has been deleted. Thus, Applicant believes that the objection under 35 U. S. C. 132 is no longer applicable.

In the Action, claims 1-20 and 27-33 are rejected under 35 U. S. C. 112, first and second paragraphs. As described above, the limitation in claim 1, 27 and 29, which was added into the claim by the amendment filed September 10, 2002 and which relates to the above-mentioned phrase, has been deleted. Thus, Applicant believes that the rejection under 35 U. S. C. 112, first and second paragraphs is no longer applicable. Thus, the rejection of claim 1-20 and 27-33 under 35 U. S. C. 112, first and second paragraphs accordingly should be withdrawn. Here, since claims 29-33 are not rejected by other basis, these claims are in condition for allowance. Further claims 5-10 and 16-20 also are not rejected by other basis, these claims should have patentable subject mater at least.

In the Action, claims 1-4, 11-15, 27 and 28 are rejected under 35 U. S. C. 103(a) as being unpatentable over Yamaha et al. in view of Hosoda et al. The rejection is respectfully traversed.

As described above, the limitation, which was added in the Amendment

filed September 10, 2002, has been deleted in claim 1, 27, and 29 as the examiner suggested because Applicant agrees that this limitation is not clearly written in the original disclosure. However, the original specification clearly discloses that a substrate includes a circuit area and a peripheral area. In other words, the substrate includes at least two areas, that is, the circuit area and the peripheral area, which is a different from the circuit area. One of the characteristics of the circuit area is that an integrated circuit is formed therein. Thus, the peripheral area does not have the characteristic that the circuit area has, and one of the characteristics of the peripheral area that the peripheral area encompasses the circuit area in which the integrated circuit is formed. Accordingly, although the limitation described above is deleted in the claims 1, 27 and 29, the peripheral area appeared in claims 1, 27 and 28 should be interpreted that the peripheral area encompasses the circuit area, which is different from peripheral area, the circuit area including the characteristic that the integrated circuit is formed therein.

Now, Referring to Yamaha et al., with respect to claim 1, the examiner asserts that (a) the peripheral area encompassing the circuit area, and (b) the first

dummy pattern (13) being formed in the dummy area (which means the peripheral area), are disclosed. **This examiner's assertion is clearly incorrect**. As described in the Paper filed September 10, 2002 on page 23 line 8 through page 25, line 1 in detail, regarding (b) mentioned above, **the dummy pattern (13) of Yamaha et al. is formed in a region where a lower layer wiring (12) is not formed closely, not in the peripheral area.** This is clear because the upper layer wiring (16), which is a part of the integrated circuit, is formed above the dummy pattern (13). Further, regarding (a) mentioned above, the examiner fails to identify the peripheral area of the Yamaha device. That is, as also described in the Paper filed September 10, 2002 on the same pages as mentioned above, the area (RB) in Fig. 5 is a part of the circuit area but the peripheral area because an upper layer wiring (16), which is a part of an active circuit, is formed over the dummy pattern (13). Thus, the area (RB) simply shows the region where the lower layer wiring (12) is not formed closely. In the past Office Action dated December 28, 2001 on page 4, lines 3 and 6, the examiner asserted that the area (RB) of Yamaha et al. is a dummy area. However, after Paper dated September 10, 2002, which includes the

explanation of what the area (RB) is, is filed, the examiner deletes the reference symbol (RB) in order to indicate the peripheral area in this Office Action. According to this fact, Applicant understands that the examiner realizes that the area (RB) is not the peripheral area. Thus, Applicants respectfully requests to indicate where the peripheral area is disclosed in Yamaha et al. For the examiner's reference, a full translation of the Yamaha reference, which is translated by the Japanese Patent Trademark Office, is attached hereto.

Next, the examiner asserts that the first dummy pattern being formed of the same material as the wiring pattern is disclosed in Yamaha, et al. **Applicant disagrees.** As the examiner can understand by reviewing the full translation of Yamaha et al, Applicant could not find any description regarding this limitation in Yamaha et al. Thus, Applicants respectfully requests to indicate where this limitation is disclosed in Yamaha et al.

The examiner asserts that the second insulating layer (14b) is not formed over the first dummy pattern (13) in Yamaha et al. As described in Paper filed September 10, 2002, **this examiner's assertion is incorrect.** It is very clear from

the attached full translation in the column [0017], which corresponds to Fig. 5, **there is a thin SOG layer formed above the dummy wiring 13**. According to the full translation, it is written that "(I)n the isolated field RB in which it is not crowded with wiring, even if the lower layer dummy wiring 13 is arranged, the silicon-oxide layer by SOG which collects on it will be thin". Thus, Yamaha does not disclose the second insulating layer being not formed over the first dummy pattern.

Furthermore, the examiner asserts that Yamaha et al. disclose a third insulating layer (14c) formed on the exposed first insulating layer (14a). As explained in detail above, there **is** a thin SOG layer(a second insulating layer) above the dummy pattern (See the column [0017] in the full translation). This means that there is the thin SOG layer (14b) on the first insulating layer (14a). Thus, after forming the SOG layer, no exposed first insulating layer exists in Yamaha device. Therefore, it is impossible for Yamaha device to protect his device from moisture, which come into the circuit area through the SOG layer (14b).

The examiner asserts that the dummy pattern (13) encompassing the circuit area (RA) is not disclosed in Yamaha et al. **Applicant agrees.** However, the

examiner also asserts that Hosoda et al. teaches that the dummy pattern (14a) can be formed any where on a chip including surrounding the circuit pattern, hence peripheral area (see Fig. 3). **Applicant disagrees.** In Fig. 3 of Hosoda et al., the dummy patterns (14a) are disposed around the wiring (13a). However, the wiring (13a) is **not surrounded** by the dummy patterns (14a). Since the dummy patterns (14a) of Hosoda are formed for purpose of the planarization, the dummy pattern (14a) can be disposed around the wiring (13a) to achieve his purpose. However, according to Hosada et al, since the dummy patterns (14a) are **studded** around the wiring (13a), the SOG layer is formed between the dummy patterns (14a). Thus, it is impossible to protect the wiring (13a) from moisture. On the other hand, according to the invention, since the dummy pattern encompasses the circuit area, it is possible to protect the IC from moisture because no SOG layer is formed on the dummy pattern, which encompasses the circuit area. It is clear from the description of the specification and the purpose of the invention that the meaning of "the dummy pattern encompassing the circuit area " should be understood that the dummy pattern surrounds the circuit area completely because if the dummy pattern

Comparison table

of the invention is formed in the way of Hosoda's disclosure (Namely, the dummy patterns (13a) are studded around the wiring (13a)), the invention can not achieve its purpose. Thus, it is clear that Hosoda et al. does not disclose the dummy pattern surrounding the circuit area.

As to the examiner's comment of "**Product by process limitation**" on the Action dated December 3, 2002, it is applying to the original claims. However, claims 3-5, 10, 14, 15, 19 and 20 had been amended dated September 10, 2002 and March 28, 2002, and these claims are directed to the product per se by the amendments. Applicants believes that the assertion by the examiner on this matter had already been overcome. Applicant respectfully requests to reconsider the examiner's assertion of this matter to the amended claims.

Therefore, since Yamaha et al. and Hosoda et al. alone or in combination neither show nor suggest the claimed characteristics as described above, which are defined in claim 1, claim 1 is deemed to be clearly patentable over Yamaha et al. in view of Hosoda et al., and the rejection of claim 1 accordingly should be withdrawn. Further, as to the dependent claims, such as claims 2-4 and claims 11-15, claims

2-4, and claims 11-15 depend from claim 1 directly or indirectly so that the rejection of claims 2-4 and claims 11-15 also should be withdrawn.

Specifically, as to claim 3, the examiner asserts that the first dummy pattern (13) of Yamaha et al. has a width. Applicant does not understand the examiner's intention. Any kinds of objects on the earth have a width. Thus, any kinds of dummy pattern have a width. The limitation of claim 3 **is not intended to** the characteristic that the first dummy pattern has a width. Rather, the limitation of claim 3 is intended to how the width of the first dummy pattern is determined. According to claim 3, the width of the first dummy pattern is determined by a concentration of solid content of the OSG layer. However, Yamaha et al. do not disclose how the width of the first dummy pattern (13) is determined.

As to claim 4, the examiner asserts the width of the first dummy pattern (13) of Yamaha et al. is designed for various size including less than 1 μm. However, Yamaha et al do not disclose that the first dummy pattern (13) is designed in a specific range including less than 1 μm. Rather, according to the Yamaha's disclosure in the column [0034], the width of the dummy wiring is set to about 8-9

μm.

As to claim 11, the examiner mentions the Lee device. Applicant understands that the Lee device should be the Yamaha device because reference numbers (13e), (13d), (12), (13a-e) and (14b) are not found in Fig. 5 of Lee. The examiner assets that a third dummy pattern (13e) is formed in the dummy area. **This is incorrect.** As described above, the third dummy pattern (13e) is formed in the circuit area as well as the first dummy pattern because the area (RB) shows the circuit area. In Fig. 6, the SOG later (14b) is formed on the third dummy pattern (13e), and the SOG later (14b) is also formed on the first dummy pattern (13) in Fig. 5 as explained above. Thus, even if the disclosure used in the Fig. 5 is applied to the device shown in Fig. 6, it is very a reasonable interpretation that the SOG layer (14b) is formed on the third dummy pattern (13e).

As to claim 12, the examiner assets that the width of the third dummy pattern (13e) of Yamaha et al. appears to be almost the same as that of the first dummy pattern (13d). However, there is no such a description in Yamaha et al. The examiner may suggest that the width of the third dummy pattern (13e) looks

equal to that of the first dummy pattern (13d) in Fig. 6. However, it is not enough to reject the claim because drawings are not required to be illustrated very accurately.

As to claim 14, the same argument as that of claim 3 is applied here.

As to claim 15, the same argument as that of claim 4 is applied here.

As to independent claim 27, the similar arguments as that of claim 1 are applied here. That is, Yamaha et al. do not disclose that (1) the a dummy pattern is formed of the same material as that of the wiring pattern, (2) the dummy pattern is formed in the peripheral area, (3) the dummy pattern encompasses the circuit area, and (4) an insulating layer is not formed over the dummy pattern while the insulating layer is formed over the wiring pattern and formed outside the dummy pattern.

The examiner also asserts that Hosoda et al. teaches that the dummy pattern (14a) can be formed any where on a chip including surrounding the circuit pattern, hence peripheral area (see Fig. 3). However, **this is incorrect** because of the reasons described above. That is, although the dummy pattern (14a) is disposed around the wiring (13a) in Hosoda device, the wiring (13a) is **not**

surrounded by the dummy patterns (14a).

Therefore, since Yamaha et al. and Hosoda et al. alone or in combination neither show nor suggest the claimed characteristics as described above, which are defined in claim 27, claim 27 is deemed to be clearly patentable over Yamaha et al. in view of Hosoda et al., and the rejection of claim 27 accordingly should be withdrawn. Further, as to the dependent claims, such as claim 28, claim 28 depends from claim 27 directly so that the rejection of claim 28 also should be withdrawn.

In view of the foregoing, the application is deemed to be in condition for allowance and such is earnestly solicited. Should any further fee be needed, please charge it to our Account No. 50-0945 and notify us accordingly.

Attached hereto is a marked-up version of the changes made to claims by the current amendment. The attached page is captioned "**Version with markings to show changes made.**"

Respectfully submitted,

Junichi MIMURA
(Registration No.40,351)
Oki America, Inc.
1101 14th Street, N.W., Suite 555
Washington, D.C. 20005
Telephone: (202) 452-6190
Telefax: (202) 452-6148
Customer No.: 26071

Date : March 3, 2003

ATTACHMENT
(1) **"Version with markings to show changes made."**
(2) Full translation of Japanese laid open patent 10-270445

VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the claims:

Claims 1, 27 and 29 have been amended as follows.

1 (3rd amended). A semiconductor device, comprising:

a semiconductor substrate having a circuit area where an integrated circuit is formed and a peripheral area ~~where an integrated circuit is not formed, the peripheral area~~ surrounding the circuit area;

wiring patterns formed on the substrate in the circuit area;

a first dummy pattern which is formed of the same material as the wiring pattern, formed in the peripheral area, the dummy pattern encompassing the circuit area;

a first insulating layer formed on the circuit area and the peripheral area of the semiconductor substrate;

a second insulating layer formed on the first insulating layer which is formed on the semiconductor substrate, wherein the second insulating layer is formed over the wiring patterns, and the second insulating layer is not formed over the first dummy pattern; and

a third insulating layer formed on the exposed first insulating layer and the second insulating layer.

27 (2nd amended). A semiconductor device, comprising:

a semiconductor substrate having a circuit area where an integrated circuit is formed and a peripheral area ~~where an integrated circuit is not formed, the peripheral area~~ surrounding the circuit area;

wiring patterns formed on the substrate in the circuit area;

a dummy pattern which is formed of the same material as the wiring pattern, formed in the peripheral area, the dummy pattern encompassing the circuit area; and

an insulating layer formed above the semiconductor substrate, the insulating layer being formed over the wiring patterns, the insulating layer being formed outside the dummy pattern but not being formed over the dummy pattern, and the insulating layer having a moisture absorbable characteristic.

29 (2nd amended). A semiconductor device, comprising:

a semiconductor substrate having a circuit area where an integrated circuit is formed and a peripheral area ~~where an integrated circuit is not formed, the peripheral area~~ surrounding the circuit area;

wiring patterns formed on the substrate in the circuit area, the wiring pattern including a pad pattern;

a dummy pattern which is formed of the same material as the wiring pattern, formed in the peripheral area, the dummy pattern encompassing the circuit area;

a first insulating layer formed over the wiring patterns and the dummy pattern, an edge of the first insulating layer being located on the pad pattern, which is adjacent the dummy pattern; and

a second insulating layer formed above the semiconductor substrate, the second insulating layer being formed over the wiring patterns and the second insulating layer being formed outside the dummy pattern but not being formed over the dummy pattern.